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10/811,407	03/26/2004	Dale W. Schroeder	10030930-1	3279

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EXAMINER	
SITTA, GRANT	
ART UNIT	**PAPER NUMBER**
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,407	SCHROEDER, DALE W.	
	Examiner	Art Unit	
	Grant D. Sitta	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Applicant has failed to include the U.S. Application Serial number for varies Applications through out the specification.

Appropriate correction is required.

Double Patenting

1. Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 7,019,879. Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicant claims "set including row-adjacent **and** column-adjacent ones of said circuit elements." A set including both row-adjacent and column-adjacent "ones" as a result at least three "ones" will be included in a group. Patent 7,019,879 teaches "a set comprising at least two of circuit elements positioned diagonally adjacent one another in array." Thus, with three circuit elements in an adjacent row and column array there must be at least one pair of circuit elements that are diagonally adjacent with one another.

2. Claims 6 and 28 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 7,019,879.

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the grouping of the circuit elements Applicant is claiming circuit elements that are both orthogonally-adjacent.

3. Claim 7 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 3 of U.S. Patent No. 7,019,879. Although the conflicting claims are not identical, they are not patentably distinct from each other because "atleast two adjacent rows" is obviously similar as "array number more than two."

4. Claim 9 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 9 of U.S. Patent No. 7,019,879. Although the conflicting claims are not identical, they are not patentably distinct from each other because both claims load data into a buffer before sending the data to the circuit elements and both depend on obviously similar claims.

Claim Objections

5. Claim 27 objected to because of the following informalities: Double commas at the end of line 2. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant claims "said buffer is configured to load data into ones of said circuit elements in at least a portion of at least two of the rows of the array." In claim 1 lines 6 Applicant refers to "said ones." It is unclear which "ones" the buffer is to load data into.

7. Claims 15-18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant refers to the "spatial light modulator" of claim 13. However, there is no mention of a "spatial light modulator" in claim 13.

8. Claims 19-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant refers to the "spatial light modulator" of claim 1. However, there is no mention of a "spatial light modulator" in claim 1.

9. Claims 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant refers to the "loading data into a first section of the array in response to a strobe signal derived from the strobe signal..." claim 32 lines 1-2. However, It is unclear how the data can be loaded in to a first section in response to a strobe signal and be derived from the same strobe signal.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1-5, and 8-10 rejected under 35 U.S.C. 102(b) as being anticipated by Bagley (3,564,510) hereinafter Bagley.

3. In regards to claim 1, circuit elements (fig. 6, (2)) arranged in an array of rows (Fig. 6, BO-R1, B1-R1, etc) and columns (Fig. 6, BO-R1,BO-R2, etc), said circuit elements (fig. 6, (117)) being alterable (col. 15, lines 10-15 "[indicators] shifted from one set to another" thus alterable.) in response to data stored (co. 10, lines 3 "latch") therein and configured to shift data (col. 15, lines 10-15, "shifted") therebetween; and a strobe line (fig. 6 (119) or line (BIT 0), (BIT 1) etc.) electrically coupled to ones of said circuit elements (Fig. 6, electrically coupled through A for (BO-R1), (B1-R1)) constituting a set (Fig. 6 BO-R1- BO-R2) (B1-R1) provide thereto a strobe signal (Fig. 6 119) to cause said ones (BO-R1), (B1-R1)) of said circuit elements (fig. 6, (2)) in said set to shift data (col. 15, lines 10-15, "shifted") to non-adjacent ones (BO-R10) of said circuit elements (fig. 6, (2)) outside said set in an interleaving pattern (col. 2, line 45 "interleaved"), said set including row-adjacent (Fig. 6, BO-R1, B1-R1, etc) and column-adjacent (Fig. 6, BO-R1,BO-R2, etc), ones of said circuit elements (Fig. 6.

4. In regards to claim 2, wherein said strobe line (BIT 0, BIT 1, etc.) is electrically coupled to ones ((B0-R1), (B0-R2), etc.) of said circuit elements (fig. 6, (2)) located in at least a portion of at least two adjacent rows (B0-R1, B0-R2) of the array.

5. In regards to claim 3, said strobe line (fig. 6 (119) or line (BIT 0), (BIT 1) etc.) is electrically coupled to ones of said circuit elements ((B0-R1), (B0-R2), etc.) located in a first pair of adjacent rows (BIT O and BIT 1) of the array to provide a first strobe signal to said ones of said circuit elements located in the first pair of adjacent rows (BIT 0 and BIT 1); and

said electronic circuit (fig. 6 (2)) additionally comprises an additional strobe line (fig. 6 ROW 2 or BIT 1) electrically coupled to ones of said circuit elements (Fig 6 (2) located in a second pair of adjacent rows (BIT 0, BIT 1, BIT 23 is connected to ROW 1, 2 -10) of the array to provide a second strobe signal (BIT 1) to said ones of said circuit elements (fig. 6 (2)) located in the second pair of adjacent rows (BIT 1 and ROW 2).

6. In regards to claim 4, the first strobe signal (BIT 0) is operable to shift data (col. 15, lines 10-15, "shifted") from said ones of said circuit elements (fig. 6 (2)) in the first pair of adjacent rows (ROW 1 and ROW 2) to said ones of said circuit elements (fig. 6 (2)) in the second pair of adjacent rows (ROW 3 and ROW 4).

7. In regards to claim 5, the strobe line (fig. 6 (119) or line (BIT 0), (BIT 1) etc.) is electrically coupled to ones of said light modulation elements (fig. 6 (2)) located in at least a portion of at least two adjacent columns of the array(fig. 6, (BIT 0), (BIT 1). Examiner notes the indicator lamp, is a light emitting element that changes according to the input. Thus, qualifies as a "light modulation element".

8. In regards to claim 8, there orthogonally-adjacent one of said circuit elements are in at least two adjacent columns (Fig. 6 B0-R2 and B1-R1 are orthogonally adjacent).

9. In regards to claim 9, a buffer (Fig. 2a (latch) col . 6 line 40-55) connected to at least one end of the array to load the data into ones of said circuit elements. (col . 6 line 40-55). Examiner notes that Fig. 2a which includes the latches is connected to the end of the array through bus lines (BIT 0, 1, etc.) into Fig. 6 (15).

10. In regards to claim 10, wherein said buffer (Fig. 2a (latch) col . 6 line 40-55) is configured to load data into ones of said circuit elements in at least a portion of at least two of the rows of the array (Fig. 6). Examiner notes the data sent on the BIT lines will load data into at least a portion of at least two of the rows.

11. In regards to claim 11, where a buffer (Fig. 2a (latch) col . 6 line 40-55) is configured to load data (col . 6 line 40-55). into ones of said circuit elements in at least a portion of at least two of the columns of the array(BIT 0, 1, etc.) into Fig. 6 (15).

12. Claims 21-23, 25, and 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Grabert et al. ((7,133,022) hereinafter Grabert.

13. In regards to claim 21,loading data (col. 4 lines 50-55, "assigned data") representing an image (col. 4 lines 50-55, "to produce an image") into light modulation elements (col. 4 lines 50-55,"light modulators"); altering (col. 4 lines 50-55, "adjusting") ones of the light modulation elements (col. 4 lines 50-55,"light modulators"); in response to the data loaded (col. 4 lines 50-55, "assigned data") thereinto to transfer an instance of the image onto a substrate (col. 4 lines 50-55, "produce image"); shifting the data between non-adjacent (col 9. lines 35-60, "remote

proxils")ones of the light modulation elements in an interleaving pattern (col. 7, lines 59-65, "interleaving"); altering ones of the light modulation elements in response to the data shifted thereinto to transfer another instance of the image onto the substrate. (col 9. lines 35-60).

14. In regards to claim 22, wherein each said altering further comprises: applying a voltage in response to the data to the change optical characteristics of the light modulation elements (col. 2, lines 62-70) "to get a very "white color from a bulb the filament must operate at a high temperature which requires higher voltages...").

15. In regards to claim 23, applying strobe signals to strobe lines electrically coupled to respective ones of said light modulation elements (proxels) to cause the data to be shifted ("a remote") between the non-adjacent ones of the light modulation elements (col. 9 lines 35-60). Examiner notes that the proxels must be attached to some form of strobe line for addressing and by using a remote pixel as show in fig. 7D to emit for the inoperable pixel the data must be shifted.

16. In regards to claim 25, providing the light modulation elements arranged in an array of rows and columns (Fig. 5A). depicting arrangement of proxels within a projection device in rows and columns.

17. In regards to claim 29, the method additionally comprises providing the light modulation elements arranged in an array of rows and columns (Fig 5A); and loading the data into the light modulation elements at one end of the array. (Fig. 15. "Data) Examiner notes the data is loaded in at one end of the array.

18. In regards to claims 30 and 31, see claim 29. Examiner notes by using a portion of two rows Applicant could use the same method as explain in claim 29.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being obvious unpatentable over Bagley.

21. In regards to claim 6, where a strobe line (fig. 6 (119) or line (BIT 0), (BIT 1) etc.) is electrically coupled to at least two groups of orthogonally-adjacent ones of said circuit elements Fig. 6 B0-R2 and B1-R1, said at least two groups being positioned diagonally in the array with respect to one another. Examiner notes it would have been an obvious matter of design choice to have at least two groups being positioned diagonally in the array with respect to one another. Such a modification would have involved a mere change in the orientation of the strobe line. A change in direction of the strobe line would generally be recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

22. In regards to claim 7, wherein said orthogonally-adjacent ones of said circuit elements are in at least two adjacent rows (Fig. 6 B0-R2 and B1-R1 are orthogonally adjacent).

23. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. Claims 12-14, 16-17, 24 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bagley in view of Grabert et al (7,133,022) hereinafter, Grabert.

25. In regards to claim 12, Bagley discloses the limitations of claim9,

Bagley differs from the claimed invention in that Bagley does not disclose a buffer that comprises different elements that load data into respective portions of the array and a clock associated with a first portion of the array to load data into the first portion of the array.

However, Grabert. teaches a system and method for a buffer (Fig. 16) comprises buffer elements (Fig 16, 370, 372, 374, clock, each of said buffer elements loading data into a respective portion of the array (Fig. 16 382, 384, 386), said strobe line being within a second portion of the array and being connected to clock (Fig. 16 Pixel clock) one of said buffer elements associated with a first portion of the array to load data into

the first portion of the array (Fig. 16 370 associated with 382). (col. 14, lines 25-70 of Grabert).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Bagley to include the use of buffer elements loading data in to portions of the array as taught by Grabert in order to higher refresh rates so that the image is crisper and less image flicker as stated in (col. 3, lines 45-60 of Grabert).

26. In regards to claim 13, memory elements (fig 16 390, 370, 372, 374 and Fig 15 342) configured to store the data and shift the data (col. 14, lines 60-70 "shift stored configuration in memory") therebetween; and pixel controllers (Fig. 15 (344)) configured to alter the state of respective ones of said light modulation elements ("Proxel") in response to the data stored ("DATA") in respective ones of the memory elements (Fig. 16 and Fig. 15 col. 14 lines 5-70) .

27. In regards to claim 14, wherein the memory elements (Fig. 16 370, 372, 374) include two groups of the memory elements (Fig 16 370, 372), the pixel controllers being (Fig. 15 (344) and Fig. 16 (368)) controlled by the memory elements (Fig 16 370, 372) in an interleaving pattern (col. 2, line 45 "interleaved") between the two groups of memory elements (370 and 372).

28. In regards to claim 16, wherein said light modulation elements comprise liquid crystal material (Fig. 12D,"Which an LCD panel layer is integrated")

29. In regards to claim 17, the pixel controllers (Fig. 15 (344) and Fig. 16 (368)) include pixel electrodes (Fig. 16 Examiner notes where two or more electronic elements meet there will be electrodes) configured to receive the data stored in the respective

memory elements (Fig. 16, 382, 384, 386) , and said light modulation elements collectively comprise a common electrode configured to receive a common electrode signal for said light modulation elements (Fig 16 Pixel Clock) .

30. In regards to claim 18, a light modulation elements (col. 4, lines 5-15) additionally include micromirrors (col. 4, lines 5-20, "mirror"), and the pixel controllers comprise electromechanical (Col. 4, lines 5-20 "micro electromechanical mirror") devices configured to control the state of said respective ones of said micromirrors (col. 4, lines 5-20, "mirror"), in response to the data stored in respective ones of said memory elements (col. 4, lines 5-20).

31. In regards to claim 19, additional strobe lines (fig. 16); and a shift register electrically (fig. 16 (390)) connected to said strobe lines to apply the strobe signals sequentially thereto. (Fig. 10A col. 37-47).

32. In regards to claim 20, wherein shift register implements a ripple clock (col. 14, lines 35-40 "pixel clock"). Examiner notes a ripple clock is an obvious choice when using multiple electronic components due to inherent time delays in electronic components.

33. In regards to Claim 24, Grabert disclosed utilizing a ripple clock to control the timing of said applying (col. 14, lines 35-40 "pixel clock"). Examiner notes a ripple clock is an obvious choice when using multiple electronic components due to inherent time delays in electronic components.

34. In regards to claim 26, applying the strobe signals to respective sets (Fig. 11 Blue, Green and Red) of the light modulation elements, at least one of the sets comprising ones of the light modulation elements (proxels) in at least a portion of at

least two adjacent rows; and shifting the data between the light modulation elements in non-adjacent rows Fig. 15 and 16 col. 14-15, lines. Examiner notes since Fig. 16 contains at least three shift lines two adjacent rows could shift the data to a third row which is not adjacent to the first.

35. In regards to claim 27, see claim 26. Examiner notes it would have been an obvious matter of design choice to shift the data to columns as apposed to rows.

36. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grabert and Bagley as applied to claim 13 above, and further in view of Page et al. (6,078,316) hereinafter Page.

37. In regards to claim 15, Grabert and Bagley discloses the limitations of 13.

Grabert and Bagley differs from the claimed invention in that Grabert and Bagley does not disclose The spatial light modulator of Claim 13, wherein each of the memory elements further includes an output node electrically coupled to the respective pixel controller and to an input node of a non-adjacent one of the memory elements.

However, Page teaches a system and method for each of the memory elements (Fig. 3 "RAM") further includes an output node electrically coupled to the respective pixel controller (Fig. 3 "refresh controller") and to an input node of a non-adjacent one of the memory elements. (col. 6, lines 35-70 of Page). Examiner notes Applicant is merely claiming a shift register.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Grabert and Bagley to include the use of shift registers as taught by

Page in order to serve as a data buffer as stated in (col. 5, lines 30-40 of Page) and also act as a delay circuit or to sequentially supply data.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

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